

AMENDMENTS TO THE CLAIMS

1. (currently amended) A programmable conductor memory cell for an integrated circuit, comprising:

a first insulating layer having a top surface and a cell body via;

a memory cell body comprising a glass electrolyte with metal ions disposed therein, the memory cell body having being formed entirely within the cell body via and defining a sidewall where the memory cell body and the first insulating layer make contact;

a cathode surface in contact with a cathode the memory cell body; and

a second insulating layer over the first insulating layer extending partially over the top surface of the memory cell body and defining an anode via to the memory cell body; and

an anode surface in contact with an anode a top surface of the memory cell body and filling a cell body- formed in the anode via in a first insulating layer, thereby defining a sidewall where the memory cell body and the first insulating layer make contact;

a second insulating layer over the first insulating layer; and

wherein the anode at least partially filling an anode via through the second insulating layer, the anode contacting only a central portion of contacts the anode top surface of the memory cell body, the central portion spaced inwardly from without contacting the sidewall of the memory cell body.

Claims 2 and 3. (canceled)

4. (currently amended) The programmable conductor memory cell of Claim 3 52 wherein the spacer comprises an insulating material.

5. (currently amended) The programmable conductor memory cell of Claim 3 52 wherein the spacer has a thickness extending into the anode via between about 5 nm and 30 nm.

6. (currently amended) The programmable conductor memory cell of Claim 3 52 wherein the spacer comprises silicon nitride.

7. (currently amended) The programmable conductor memory cell of Claim 1 wherein the memory cell body ~~second insulating layer~~ comprises ~~silicon nitride~~ a plurality of layers.

8. (original) The programmable conductor memory cell of Claim 1 wherein the anode via is filled with metal.

9. (currently amended) The programmable conductor memory cell of Claim 8 wherein the metal in the anode via is contiguous with a metal layer over the second insulating layer.

10. (original) The programmable conductor memory cell of Claim 1 wherein the cathode comprises tungsten.

11. (currently amended) The programmable conductor memory cell of Claim 1 wherein the memory cell body comprises a chalcogenide-metal ion glass electrolyte material.

12. (original) The programmable conductor memory cell of Claim 11 wherein the metal ions are chosen from the group consisting of silver, copper, zinc and combinations thereof.

13. (original) The programmable conductor memory cell of Claim 11 wherein the anode comprises silver.

14. (original) The programmable conductor memory cell of Claim 13 wherein the glass electrolyte material comprises silver-germanium-selenium.

15. (currently amended) The programmable conductor memory cell of Claim 1 wherein a distance between ~~the cathode~~ a bottom surface and the ~~anode~~ top surface of the memory cell body is about 25 nm to 100 nm.

16. (original) The programmable conductor memory cell of Claim 1 wherein a width of the memory cell body via is between about 100 nm and 500 nm.

17. (original) The programmable conductor memory cell of Claim 1, wherein a width of the memory cell body via is between about 200 nm and 300 nm.

18. (original) The programmable conductor memory cell of Claim 1, wherein the first insulating layer comprises silicon nitride.

19. (original) The programmable conductor memory cell of Claim 18, wherein the first insulating layer has a thickness between about 10 nm and 200 nm.

20. (original) The programmable conductor memory cell of Claim 18, wherein the first insulating layer has a thickness between about 25 nm and 150 nm.

21. (original) The programmable conductor memory cell of Claim 1, wherein the second insulating layer comprises silicon nitride.

22. (currently amended) The programmable conductor memory cell of Claim ~~20~~ 21 wherein the second insulating layer has a thickness between about 50 nm and 200 nm.

23. (currently amended) The programmable conductor memory cell of Claim ~~20~~ 21, wherein the second insulating layer has a thickness between about 80 nm and 150 nm.

24. (currently amended) The programmable conductor memory cell of Claim ~~1~~ 52 wherein the anode via has a width no greater than a width of the cell body via.

Claims 25-48. (canceled)

49. (new) The programmable conductor memory cell of Claim 1, wherein the memory cell body fills the cell body via.

50. (new) The programmable conductor memory cell of Claim 1, wherein the top surface of the memory cell body is coplanar with the top surface of the first insulating layer.

51. (new) The programmable conductor memory cell of Claim 1, wherein the cathode extends outside the sidewall of the memory cell body.

52. (new) A programmable conductor memory cell for an integrated circuit, comprising:
a first insulating layer having a top surface and a cell body via;
a memory cell body comprising a glass electrolyte with metal ions disposed therein, the memory cell body being contained within the cell body via and defining a sidewall where the memory cell body and the first insulating layer make contact;
a cathode in contact with the memory cell body;
a second insulating layer over the first insulating layer and defining an anode via to the memory cell body;
an anode in contact with a top surface of the memory cell body and formed in the anode via;
wherein the anode via has a width about the same as a width of the memory cell body, and the anode via is lined with a spacer that covers a sidewall edge of the memory cell body, such that the anode contacts the top surface of the memory cell body without contacting the sidewall of the memory cell body.

53. (new) The programmable conductor memory cell of Claim 52, wherein the anode via is filled with metal.

54. (new) The programmable conductor memory cell of Claim 52, wherein the cathode comprises tungsten.